# Appendix A: AMBA Protocol Support

This appendix describes support in NetSpeed Gemini for **AMBA AXI and ACE Protocol Specification Rev E.**

## ACE / AXI4 Feature Adoption

The table below provides a high level summary of ACE / AXI4 features supported by NetSpeed AXI NoC.

|  |  |
| --- | --- |
| ACE/AXI4 Feature | NetSpeed AMBA NoC Support |
| READY/VALID  Handshake | Full forward and reverse direction flow control of AMBA protocol-defined READY/VALID handshake. |
| Transfer Length | Non-coherent transactions support   * 1 to 256 beats for incrementing bursts and * 2 to 16 beats for wrap bursts. * If width conversion is needed, these requirements must hold even on the width converted requests.   Coherent ACE agents must use 64B cacheline sized and aligned transactions |
| Data Width | Agents can have data widths of 32, 64, 128, 256 and 512 bits.  R channel and W channel must have equal data size. |
| Transfer Size | Narrow transactions are fully supported |
| Burst type | WRAP requests must be 16B, 32B or 64B for non-coherent transaction. Coherent WRAP transactions must be sized to 64B cacheline. FIXED transactions are supported by splitting them into multiple single beat INCRs |
| Long bursts | Long transactions may be split into multiple transactions at a configurable boundary. Non coherent transactions will be split at 1024B boundaries by default. Coherent transactions from ACE and ACE-lite agents are split at 64B boundary. |
| Read/Write only | The IP supports only read/write mode. Read-only or write-only interfaces are not currently supported. |
| Exclusive Access | NetSpeed AMBA NoC can pass exclusive access transactions across a system. AXI4 does not support locked transfers  Note that an exclusive access burst of 128B must not be performed on master bridges might split at 64B boundary. Exclusive access sent to an AXI3 slave must not violate the maximum transfer size supported by the interface. |
| Cache bits | NetSpeed AMBA NoC passes cache bits across a system.  Cache Bit [1] can mark transaction as modifiable or non-modifiable. Modifiable transactions provide greater flexibility in the NetSpeed AXI NoC to transport and modify transactions passing through the system for greater performance. Non-modifiable transactions are honored, however some transaction marked as non-modifiable will still be subjected to modification, for example if width conversion operation requires that for functional correctness. |
| Protection bits | NetSpeed AMBA NoC passes protection bits across a system  Access control to address ranges can be configured to use the transaction’s protection bits |
| Quality of Service (QoS) Bits | NetSpeed AMBA NoC passes QoS bits across a system. QoS bits are also used for priority and weight assignments within the NoC. |
| REGION Bits | NetSpeed NoC generates region bits as part of address lookup and transports it. These regions bits are specified as part of user configuration of the address ranges. External REGION bits from a master is dropped. |
| User Bits | NetSpeed AXI NoC passes user bits across a system. The facility to transport user bits around a system allows special purpose custom systems to be built that require additional transaction-based sideband signaling. An example use of USER bits would be for transferring parity or debug information. |
| Read Interleaving | If interleaved read responses are expected from a slave, then a de-interleaving block should be added on the corresponding slave bridge. Transactions to slave supporting read interleaving will be split at 64B boundaries. Masters supporting interleaved read responses can enable the NoC to interleave responses of split segments of a read transaction. |
| Agents | Fully coherent and IO coherent agents are supported |
| Barriers | Both memory and synchronization barriers are supported |
| DVM | NetSpeed NoC supports DVM transactions for maintenance of a virtual memory system. Both DVMv7 and DVMv8 versions are supported. |
| Snoop Filter | Optional external snoop filtering is supported |
| Reset | NetSpeed AMBA NoC generally resets all VALID outputs within 16 cycles of reset, and has a reset pulse width requirement of 16 cycles or greater.  Holding AXI ARESETn for 16 cycles of the slowest AXI clock is generally a sufficient reset pulse width for NetSpeed AXI NoC. |

## AMBA Signal Adoption

The tables below provide a high level summary of AMBA signals supported by NetSpeed AXI NoC.

### Global AXI Signals

|  |  |  |
| --- | --- | --- |
| Signal | ACE |  |
| ACLK | AXI port clock | |
| ARESETn | Active low reset | |

### Write Address Channel Signals

|  |  |
| --- | --- |
| Signal | ACE |
| AWID | Fully supported.  System AID width is equal to widest AID among master interface ports. On slave interface ports, AID width can be equal, greater or less than system AID width. Masters need only output the set of ID bits that it varies (if any) to indicate re-orderable transaction threads. Masters do not need to output the constant portion that comprises the Master ID, as this is appended by the NetSpeed NoC. |
| AWADDR | Fully supported. On Master and slave ports, address width can be greater or less than system address width. Range of supported address widths is 14 to 60-bits. |
| AWLEN | Non-Coherent transfers support bursts:   * Up to 256 beats for incrementing (INCR). * Up to 16 beats for WRAP. |
| AWSIZE | Transfer width 8 to 512 bits supported. |
| AWBURST | INCR and WRAP fully supported.  FIXED transactions are split into multiple single beat INCRs |
| AWLOCK | Exclusive access supported |
| AWCACHE | NetSpeed AXI NoC will pass Cache bits across a system. Signal bits can be selectively overridden on master or slave port bridge |
| AWPROT | NetSpeed AXI NoC passes Protection bits across a system. Signal bits can be selectively overridden on master or slave port bridge. Can be used for access control. |
| AWQOS | NetSpeed AXI NoC passes QoS bit across a system. QoS bits are also used for priority and weight assignments for flows |
| AWREGION | Supported. This input is unused on the master port interface and is configured to be generated as part of address lookup |
| AWUSER | User bits per AW transaction is transported across NoC to the destination. If an AW transaction is split into multiple transactions, then user bits of the original request is repeated for each of the resultant transaction. |
| AWSNOOP | All coherent, IO coherent and non-coherent write transactions are supported. WriteUnique transactions from ACE master agents cannot cross a 64B boundary |
| AWDOMAIN | All shareability domains supported |
| AWBAR | Write barriers fully supported |
| AWUNIQUE | Optionally supported for agents requiring WriteEvict |
| AWVALID | Fully supported. |
| AWREADY | Fully supported. |

### Write Data Channel Signals

|  |  |
| --- | --- |
| Signal | ACE |
| WDATA | 32, 64, 128, 256, 512 bit widths supported. |
| WSTRB | Fully supported. |
| WLAST | Fully supported. |
| WUSER | Number of user bits per byte of the interface can be configured. This is transported across the NoC |
| WVALID | Fully supported. |
| WREADY | Fully supported |

### Write Response Channel Signals

|  |  |
| --- | --- |
| Signal | ACE |
| BID | Fully supported.  See AWID for more information. |
| BRESP | Fully supported. For an AW requests which had been split into multiple AW requests, any change in write response between individual split segments results in SLVERR write response being sent to master. |
| BUSER | User bits are defined per B response transaction. For an AW request which had been split into multiple AW requests, user bits associated with write response of first split AW segment is delivered as the BUSER bits of the entire command. BUSER of subsequent segments are ignored. |
| BVALID | Fully supported. |
| BREADY | Fully supported. |

### Read Address Channel Signals

|  |  |  |
| --- | --- | --- |
| Signal | ACE | |
| ARID | Fully supported.  System AID width is equal to widest AID among master interface ports. On slave interface ports, AID width can be equal, greater or less than system AID width. Masters need only output the set of ID bits that it varies (if any) to indicate re-orderable transaction threads. Masters do not need to output the constant portion that comprises the Master ID, as this is appended by the NetSpeed NoC. | |
| ARADDR | Fully supported. On Master and slave ports, address width can be greater or lesser than system address width. Range of supported address widths is 14 to 60-bits. | |
| ARLEN | Non-Coherent transfers support bursts:   * Up to 256 beats for incrementing (INCR). * Up to 16 beats for WRAP. | |
| ARSIZE | Transfer width 8 to 512 bits supported. | |
| ARBURST | INCR and WRAP fully supported.  FIXED transactions are split into multiple single beat INCRs | |
| ARLOCK | Exclusive access supported | |
| ARCACHE | NetSpeed AXI NoC will pass Cache bits across a system. Signal bits can be selectively overridden on master or slave port bridge | |
| ARPROT | NetSpeed AXI NoC passes Protection bits across a system. Signal bits can be selectively overridden on master or slave port bridge. Can be used for access control. | |
| ARQOS | NetSpeed AXI NoC passes QoS bit across a system. QoS bits are also used for priority and weight assignments for flows | |
| ARREGION | | Supported. This input is unused on the master port interface and is configured to be generated as part of address lookup |
| ARUSER | User bits per AR transaction is transported across NoC to the destination. If an AR transaction is split into multiple transactions, then user bits of the original request is repeated for each of the resultant transaction. | |
| ARVALID | Fully supported. | |
| ARREADY | Fully supported. | |
| ARSNOOP | All coherent, IO coherent and non-coherent read transactions are supported. ReadOnce transactions from ACE master agents cannot cross a 64B boundary | |
| ARDOMAIN | All shareability domains supported | |
| ARBAR | Read barriers fully supported | |

### Read Data Channel Signals

|  |  |
| --- | --- |
| Signal | ACE |
| RID | Fully supported.  See ARID for more information. |
| RDATA | Data widths of 32, 64, 128, 256 and 512 bits supported |
| RRESP | Fully supported. If a change in read response is detected between beats of a read response, subsequent beats are marked with SLVERR |
| RLAST | Fully supported. |
| RUSER | RUSER bits have two parts, one part defined per byte of the interface and second defined for the entire R response transaction  For an AR request which had been split into multiple AR requests, user bits associated with read response of first split AR segment is delivered as the per transaction part of RUSER bits for the entire command. Per transaction RUSER bits of subsequent segments are ignored. |
| RVALID | Fully supported. |
| RREADY | Fully supported. |

### Snoop Address Channel Signals

|  |  |
| --- | --- |
| Signal | ACE |
| ACADDR | Supported on coherent ACE agents and DVM master agents |
| ACSNOOP | Supported on coherent ACE agents and DVM master agents |
| ACPROT | Supported on coherent ACE agents and DVM master agents |
| ACVALID | Supported on coherent ACE agents and DVM master agents |
| ACREADY | Supported on coherent ACE agents and DVM master agents |

### Snoop Response Channel Signals

|  |  |
| --- | --- |
| Signal | ACE |
| CRRESP | Supported on coherent ACE agents and DVM master agents |
| CRVALID | Supported on coherent ACE agents and DVM master agents |
| CRREADY | Supported on coherent ACE agents and DVM master agents |

### Snoop Data Channel Signals

Snoop data (CD) channel is optional on an ACE agent. This channel is also not supported on DVM only master agents. If present, CDDATA width can be configured independent of the agent’s AXI data width

|  |  |
| --- | --- |
| Signal | ACE |
| CDDATA | Optionally supported on coherent ACE agents |
| CDLAST | Optionally supported on coherent ACE agents |
| CRVALID | Optionally supported on coherent ACE agents |
| CRREADY | Optionally supported on coherent ACE agents |

### Acknowledge Channel Signals

|  |  |
| --- | --- |
| Signal | ACE |
| RACK | Read acknowledge supported from coherent ACE agents |
| WACK | Write acknowledge supported from coherent ACE agents |

## AXI4-Lite Feature Adoption

|  |  |
| --- | --- |
| AXI4 Lite Feature | NetSpeed AXI NoC Support |
| Ports | AXI4-Lite master and slave ports can connect to NetSpeed AXI NoC. Intercommunication between AXI4 agents and AXI4-Lite agents is supported, conversions are performed by the NoC |
| Conversion | INCR transactions of length > 1 from AXI masters to AXI4-Lite slaves, are split into multiple AXI4-Lite transactions of 32-bit or 64-bit size. Responses from the slave are converted back to the format expected by the AXI master. WRAP requests sent to an AXI4-Lite slave will result in a SLVERR response |
| Transfer Length | AXI4-Lite is restricted to single beat transactions |
| Data Width | 32-bit and 64-bit AXI4-Lite interfaces are supported |
| Address Width | Support range of address width is 14-bit to 60-bits |
| Transfer size | AXI4-Lite does not support narrow transfers and all transactions are of full data width |
| AID | No ID bits are present in AXI4-Lite. Multiple outstanding transactions are supported; however, all transactions must be ordered. |

## AXI3 Feature Adoption

|  |  |
| --- | --- |
| AXI3 Feature | NetSpeed AXI NoC Support |
| Transfer Length | Burst length is restricted to the range 1 to 16 beats |
| Splitting | If a transaction from an AXI4 master would exceed ALEN on an AXI3 slave port, then the transaction is split into multiple transactions at 16 beat boundaries. |
| WID | This signal is available on the W data channel interface. However, write interleaving is not supported |
| AxLOCK[1:0] | AXI3 locked transactions are not supported and are converted to Normal transactions |

## AHB-Lite Feature Adoption

|  |  |
| --- | --- |
| AHB-Lite Feature | NetSpeed AXI NoC Support |
| Version | AHB-Lite master and AHB-Lite slave devices can connect to NetSpeed AXI NoC. |
| Data Width | 32, 64, 128 bits |
| Address Width | Range of 14 – 60 bits |
| HPROT | HPROT[0] maps to AxPROT[2] after logic inversion (due to polarity   change)  HPROT[1] maps to AxPROT[1]  HPROT[2] maps to AxCACHE[0]  HPROT[3] maps to AxCACHE[3], AxCACHE[2] and AxCACHE[1]   after logic duplication |
| HSIZE | 8, 16, 32, 64, 128-bit transfer size |
| HMASTLOCK | Locked transfers are not supported. HMASTLOCK will be ignored. |
| HBURST | All standard specified modes supported. INCR (Incrementing burst of unspecified length) is split at 64B boundary. |
| HSELx | Up to 16 AHB-Lite slaves can connect to an AHB-Lite slave bridge of the NoC. Slaves on a given slave bridge can have different address and data width but common endian format |
| Response delay | On AHB-Lite master, bufferable transactions will be provided early response and non-buffer transactions will receive response from the end point. |
| Endian format | Each AHB-Lite interface on NetSpeed NoC can be configured to handle little endian or big endian format |
| Write strobes | AHB-Lite interface does not support write strobes. However, write transactions from AXI masters to AHB-Lite slaves can use partial write strobes. Empty write strobes result in no AHB access and OK response. |
| Address alignment | AXI masters can perform write accesses to AHB slaves with any address alignment. Read transactions from AXI masters with unaligned addresses are changed to aligned addresses. Read is performed to the aligned address and response can optionally be marked with SLVERR based on a programmable register bit. |

## APB Feature Adoption

|  |  |
| --- | --- |
| APB Feature | NetSpeed AXI NoC Support |
| Version | APB 2/3/4 slaves can be connected to NetSpeed AXI NoC |
| Conversion | INCR transactions from AXI masters are broken down into multiple single beat APB transactions at APB slave bridge. Responses from the slaves are converted back to the format expected by the AXI master. WRAP requests sent to an APB slave will result in a SLVERR response |
| Data Width | 32-bit APB slave devices are supported |
| Address Width | Address is fixed at 32-bit |
| PSELx | Up to 16 APB slave devices can be connected to single APB slave bridge.  Each APB slave is identified by a REGION associated with its address range |
| PREADY | Supported on APB 3, 4 slaves to allow slave to extend an APB transfer |
| PPROT | Supported on APB 4 slaves |
| PSLVERR | Supports slave error from APB 3, 4 slave devices and remaps appropriately to response sent back to master |
| Address alignment | All read transaction address from AXI masters to APB slaves must be aligned to 32-bits  Narrow read or write transactions sent to APB slave are modified to be full prior to conversion to APB, i.e. any AxSIZE from masters is changed to 2  Write transaction address to APB 2, 3 slaves must be aligned to 32-bit (unaligned access results in SLVERR response).  APB 4 slaves can be sent unaligned write transaction addresses. |
| PSTRB | Supported on APB 4 slaves to allow partial byte updates during write transfers.  Write transactions from AXI masters to APB 2, 3 slaves must not use partial write strobe. Partial write strobes result in SLVERR response?  Empty write strobes result in no access and OK response. |